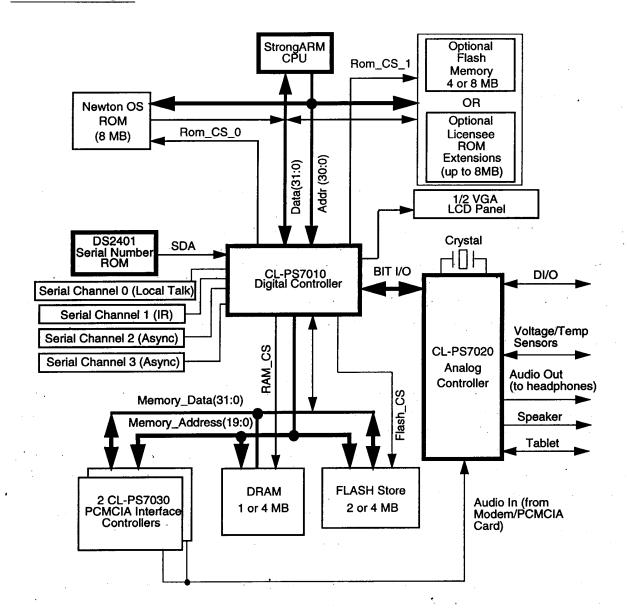
Introduction

N2 is a low-cost, low-power, high performance Personal Communicator or Personal Digital Assistant (PDA) system based on the Apple Newton architecture. This document describes the specific N2 Hardware implementation of this architecture. The N2 implementation is comprised of the following components:

- The Digital Equipment Strong Arm CPU, running at either 100 or 160 MHz
- The Cirrus Logic CL-PS-7010 Digital PDA Controller
- The Cirrus Logic CL-PS-7020 Analog PDA Controller
- Two Cirrus Logic CL-PS-7030 PCMCIA Controllers
- The Crystal Semiconductor CS8130 Infrared Transmitter/Receiver
- The Dallas Semiconductor DS2401 Serial Number ROM
- 8 or 16 Megabytes of Burst Mode Read Only Memory
- Either 2 or 4 Mbytes of Intel 28F016 FLASH Memory
- Either 1 or 4 Mbytes of Dynamic Random Access Memory
- A Resistive Tablet Pen Screen
- A A 320x480 Liquid Crystal Display panel

A block diagram of the N2 is shown in Figure 1-1.

Figure 1-1 Functional Block Diagram of the N2



Before You Continue

To use this manual effectively, you need to understand two important facets of the N2 architecture: The first is that primary control of the device resides with the Digital Controller, rather than with the CPU. The second facet is that control of some key functions is shared by more than one primary logic component, instead of residing with a single one.

This manual mirrors the architecture it supports, in that the Digital Controller is described first, and in more detail than the CPU or the other controllers. Also,

descriptions of some of the shared operations are treated as though they are equivelent to the primary logic components.

N2 Connectors

The N2 device has both external and internal connectors, allowing you to customize the device to increase, configure or modify existing functionality. External connectors are those that are accessible from outside the N2's case. Internal connectors require that you remove the case.

External Connectors

An external 26-pin D Shell Connector provides docking capabilities and is described in detail in Chapter X, "Newton Interconnect Designer's Guide." This connector provides access to two serial channels, one at RS-422 levels and the other at CMOS levels. It also allows the system to be powered externally, enables the batteries to be charged (if rechargeable NiH batteries are used), and provides for Audio input/output.

Two industry-standard Type 2 PCMCIA slots are also provided (more about these later).

An external AC adaptor powers the unit and charges the optional NiH batteries. This adapter is described in Chapter X, "Battery and Power Source."

Internal Connectors

A two-pin internal speaker connector allows an internal speaker to be connected and is described in Chapter X, "Main Logic Board Customization."

A second two-pin connector allows an internal microphone to be connected and is described in Chapter X, "Main Logic Board Customization."

A 32-pin connector allows an internal serial device to be attached and provides three serial channels (0, 2 and 3) at CMOS levels. Raw, unfused battery voltage is available, along with 3.3V, 5V and 12V. An internal line is available if a speaker is used with the internal modem. This connection is described in Chapter X, "Internal Slot Designer's Guide."

A 72-pin SIMM ROM Board slot allows increased Licensee ROM Extensions, as well as additional user storage FLASH and Internal I/O devices. This connector is described in Chapter X, "ROM Board Designer's Guide."

N2 Data Paths

This section describes the interaction of the components on the N2's main logic board.

The StrongARM CPU interfaces directly to the Digital Controller via the CPU bus. The StrongARM's internal core can operate at either 100 or 162 Mhz, selectable at manufacturing, while the bus interface operates at 12.5 Mhz.

A subset of the CPU bus, plus control signals from the Digital Controller, are available on the internal 72-pin ROM Board Connector. This connector attaches the Newton OS ROM devices, optional Licensee ROM devices, optional I/O devices and optional additional Flash devices to the system.

Balance to be supplied.

CL-PS-7010 Digital Controller

The Digital Controller contains the following subsystems:

- Memory Control
- DMA Subsystem
- Interrupt Control
- LCD Controller
- Serial Communications
- General Purpose I/O
- Timer
- Power Management

Brief descriptions of each of these subsystems follow.

The Memory Control Subsystem provides a separate Memory bus for the direct connection of DRAM and Flash devices. The Memory Bus also connects the Digital Controller to the two PCMCIA Controllers.

The Memory Subsystem can be manufactured with different DRAM and FLASH options. The Main Logic Board has sites available to support either 1 or 4 Mbytes of DRAM, and either 2 or 4 Mbytes of FLASH.

The DMA Subsystem has a centralized, fixed-priority, 8-Channel DMA Controller. DMA operations can be performed on Audio, PCMCIA, Serial Communications, External I/O, and Memory.

The Interrupt Control Subsystem supports interrupts from the following subsystems: Serial Communications, DMA Controller, Timers, General Purpose IO, and Power Management, as well as from External I/O devices, the Analog Controller, and the PCMCIA slots. All interrupts can be programmed to cause the system to wake up.

The LCD Controller generates control and data signals that support the direct connection of STN Single-Scanned and Dual-Scanned Panels in resolutions of up to 640x480, with 16 levels of gray. The N2 device provides a 20-pin pressure-fit flex cable connection to the LCD Controller Subsystem, allowing easy attachment of LCD panels. The standard N2 has a 320x480, 8-bit single-scan LCD with soft icons and supports 16 levels of gray.

The Serial Communications Controller (SCC) logic supports four serial channels (Channels 0 -3).

Channel 0 is a high-speed interface, capable of speeds of 230.4Kbits/sec when clocked internally and speeds of 2.0Mbits/sec with external clocking. Channel 0 is connected at CMOS levels to the 32-pin internal connector, and also connected externally through a LTC1323 line driver, providing RS-422 levels on the 26-pin external Newton Interconnect Connector.

Channel 1 provides a low-speed, asynchronous link for IR communication and is connected to the CS8130 IR Transceiver. The IR Transceiver supports IrDA, HPSIR, ASK & TV remote encoding/decoding. The CS8130 is connected to a external PIN diode and two transmit LEDs.

Channel 2 provides a general purpose low-speed channel, capable of speeds of up to 19.2K bits/sec. Channel 2 is also connected internally to the 32-pin internal connector.

Channel 3 provides a channel for modem communications and is capable of speeds of 38.4Kbits/sec. Channel 3 is connected to the 32-pin internal connector at CMOS levels and also to the 26-pin external Newton Interconnect Connector.

The Digital Controller has ten General Purpose I/O ports. The N2 dedictes these lines to controlling the power supply, and detecting various switches and conditions in the system.

The Digital Controller interfaces to the Analog Controller through the five-wire, serial Bit I/O bus.

CL-PS-7020 Analog Controller

The Analog Controller is comprised of the following subsystems:

- Tablet Interface
- Battery & Temperature Monitoring
- Clock Generation
- Audio
- Digital I/O

A description of each of these subsystems follows.

The Tablet Interface subsystem connects the resistive tablet through a four-wire pressure fit interface connection. The resistive tablet consists of two layers of Indium Tin Oxide (ITO). One layer is deposited on the outside of the glass that protects the LCD, and the other layer is deposited on the underside of a flexible membrane. The membrane is positioned over the glass, when the pen is applied, the two layers of ITO are connected at the point of contact made by the pen. The Tablet Interface may be converted and read by the Analog Controller's 12-bit A/D converter.

The Battery & Temperature Monitoring Subsystem utilizes the same 12-bit A/D convertor used by the Tablet Interface. The Analog Controller supports the measurement of two battery voltage levels by using two measurement channels. One channel is used to measure the battery voltage in the main batteries. The other channel measures the

voltage of the AC Charging adaptor, from either the external two-pin AC Adaptor plug or the internal charging signals from the 32-pin internal connector.

Temperature is monitored by measuring the voltage across a thermister. System temperature is checked at two locations, using dual measurement channels similar to those used by the battery monitoring logic. One channel measures the ambient temperature, while the other measures the temperature of the batteries and is used in the battery charging algorithm.

The Audio Subsystem supports both Audio-In and Audio-Out. Audio-In is selectable between two channels. One channel is connected to the internal two-pin Microphone Connector. The other channel is connected to the external, 26-pin Newton Interconnect Connector. The selected channel is connected to an internal 12-bit A/D convertor, whose output can be accessed by the Digital Controller.

The Audio-Out section combines analog data from both PCMCIA cards with data from the internal 32-pin modem connector. The data is then mixed and digitally converted. The output from this stage, along with any stream coming from the Digital Controller over the BIT I/O bus, is passed to a 12-bit D/A converter with mixer. The mixed stream is then driven to both the internal two-pin speaker connector and to the external 26-pin Newton Interconnect Connector.

The Digital I/O subsystem contains six additional signals which can be used as inputs or outputs. The N2 uses these signals for: battery monitoring, the PCMCIA voltage enable line, to reset the IR transceiver, to sense whether or not rechargeable batteries are in the unit, and to determine if a dock is attached to the external Newton Interconnect Connector. The last digital I/O line is left available for general use on the 32-pin internal connector.

StrongARM CPU

Section to be supplied.

Newton Architecture Components

This section provides detailed descriptions of each of the principal Newton Architecture components used in the N2 platform, their configuration and their interaction with the rest of the system.

The StrongARM RISC Microprocessor

The Apple Newton Architecture requires a single ARM CPU. The N2 platform uses the DEC StrongARM CPU. The following sections provide general information about the StrongARM CPU and how it is used in the N2 system. Please refer to the DEC DC1035 StrongArm RISC Processor Data Sheet for more detailed information about the functionality of the CPU.

The StrongARM is a general-purpose 32-bit microprocessor with 16 KB of data cache, 16 KB of instruction cache, memory, awrite buffer, and a memory management unit, all combined on a single chip. The StrongARM offers high level RISC performance, yet its fully static, low power CMOS design ensures minimal power consumption, making it ideal for portable, low-cost systems.

The architecture of the StrongARM is RISC based, simplifying the instruction decode. The instruction set is comprised of eight basic instruction types:

- Two types make use of the on-chip arithmetic logic unit, barrel shifter and multiplier to perform high-speed operations on the data bank of 31 registers.
- Three types of instruction control the data transfer between memory and the registers: one optimized for flexibility of addressing, another for rapid context switching, and the third for swapping data.
- Two instruction types control the flow and privilege level of execution.
- One type accesses the privileged state of the machine.

The bus interface is designed to allow the performance potential to be realized without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic.

A functional block diagram of the StrongARM processor is shown in Figure 1-2.

TCK_BYP nR/W TDI ABE CLK nBLS(3:0) **TMS** SnA **CLF** nTRST A(31:0) **nMCLK** MAS TCK TDO **MCLK APE** ⊢ nWAIT JTAG Test - TESTCLK Address Buffer CCCFG Clock MCCFG Instruction nRESET_OUT 16KByte PC MSF Cache **nMREQ** ARM SEQ CPU ADDR nRESET 16KByte **CONFIG** Data Control Cache nPWRSLP **ABORT** nIRQ Write Buffer Load/Store Data DBE D(31:0)

Figure 1-2 StrongARM RISC Processor Functional Block Diagram

StrongArm Configuration Options

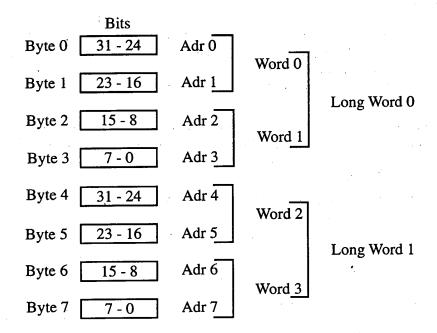
The operation and configuration of the StrongARM is controlled directly by the coprocessor instructions and indirectly via the MMU page tables. The coprocessor instructions manipulate various on-chip registers that control the configuration of the Cache, the write buffer, and the MMU, as well as a number of other configuration options. The following sections detail the how the ARM architecture options, implemented by the StrongArm, are used in the N2 system.

Big Endian

The StrongArm views memory as a linear collection of bytes numbered upwards from zero. Bytes 0 to 3 hold the first word, bytes 4 through 7 hold the second and so on.

The N2 platform configures the StrongArm to operate in Big Endian Mode. In this mode, the most signifigant byte of a word is stored at the lowest numbered byte and the least signifigant byte is stored at the highest numbered byte. Byte 0 of the memory system should be connected to data lines 31 through 24.

Figure 1-3 Figure showing how Strong Arm views Memory.



Instruction Cache

The StrongARM's 16-KByte instruction cache (IC) has 512 lines of 32 bytes (8 words) arranged as a 32-way associative cache, and uses the virtual addresses generated by the

processor core. The IC is always reloaded a line at a time (8 words). Once the line is placed in the cache, replacement will occur in round-robin fashion.

Data Cache

The StrongARM's 16-KByte data cache (DC) has 512 lines of 32 bytes (8 words) arranged as a 32-way associative cache, and uses the virtual addresses generated by the processor. The DC is always reloaded a line at a time (8 words). Replacement in the cache bank is performed using a round-robin replacement algoritym.

Write Buffer

The StrongArm write buffer is provided to improve system performance. The write buffer can handle up to eight blocks of data, from 1 to 16 bytes, at independent addresses.

There are three different types of write operation:

- a write to a bufferable and cachable location
- a write to a bufferable and noncachable locatio
- an unbuffered write

Writes to a Bufferable and Cachable Location

When writing to a Bufferable and Cachable Location, the Data Cache is first checked to see if the data is in the cache. If the data is present, the CPU performs the write to the data cache and marks the cache line as dirty, forcing it to be written to memory. By checking for data in the data cache, the StrongArm effectively increases the size of the Write Buffer.

If the data is not in the cache, the data is placed in the write buffer and the CPU continues execution, unless the Write Buffer is full. If the buffer is full, the CPU is stalled until there is sufficent space in the Write Buffer. The data is actually written at a later time to memory.

Because the N2 platform configures the StrongArm CONFIG signal to be deasserted, previous data will not be checked to see if the data being currently written is the same 16 byte area of the previous write to merge the new data with the previous write.

Writes to a Bufferable and Noncachable Location

When a bufferable write is performed to a non cacheable location, the data will be placed in the Write Buffer and the CPU continues execution, unless the Write Buffer is full. If the Write Buffer is full, the CPU stalls until sufficent space is available in the Write Buffer for the data to be written. The data is actually written at a later time to memory. Each write takes its own Write Buffer entry.

Unbuffered Writes

If the write buffer is disabled, or the CPU performs a write to an unbufferable area, the CPU will stall for several clock cycles until the write buffer empties or until the write completes externally.

Memory Management Unit

StrongARM's memory management unit (MMU) uses two 32-entry, fully associative, translation buffers (TBs) to implement standard ARM memory management functions. One TB is used for instruction access and the other for data accesses. A TB miss causes the translation table hardware to retrieve the translation and access permission information. If the entry maps to a valid Page or Section, the retrieved information is placed in the TB. An invalid Page or Section generates an abort. The TB replacement algorithm is round robin.

The MMU supports memory accesses based on both Sections and Pages. Sections are 1 Mbyte blocks of memory. Two different pages sizes are supported: Small and Large. Small pages are 4 Kbytes of memory and Large pages are 64 Kbytes of memory.

The MMU also supports the concept of domains. Domains are areas of memory that can be configured with individual access rights. The Domain Access Control Register is used to specify access rights for up to 16 separate domains.

The MMU can generate four separate faults: Alignment, Translation, Domain, and Permission. Alignment faults are generated by word loads or stores with the low-order two address bits not zero. Translation faults are generated when an invalid page is accessed. Domain and Permission faults result when you attempt a memory access that is disallowed by the current mode, domain, and page protection. Additionally, an external abort pin controlled by the Digital Controller can flag an error on an external memory access. Refer to the Digital Controller Section for more information on the use of the ABORT signal.

StrongARM Clocking

The StrongARM processor operates in one of three modes: CPU Normal, CPU Idle, and CPU Sleep. In CPU Normal mode, the processor can execute instructions. In CPU Idle mode, no instructions are executed, but the internal phase-locked loop (PLL) continues to run. In CPU Sleep mode, core power is turned off, no instructions are executed, and the PLL is off. I/O power is used to hold the output pins at the correct levels.

The processor receives a 3.68 MHz clock signal from the Analog Controller. The internal PLL locks to the input clock signal and multiplies the frequency to produce a high-speed core clock (CCLK). There are two clocking domains in the StrongArm, the core logic domain clocked by DCLK and the bus interface domain, clocked by MCLK. DCLK switches from being driven by the high speed core clock, CCLK and the bus clock MCLK.

CCLK is used as DCLK by StrongArm, except when the StrongARM is waiting for fills to complete after a cache miss. During this time, MCLK is used as DCLK.

The N2 platform configures StrongARM bus to be driven by an external MCLK, generated by the Digital Controller. To accomplish this, the N2 platform configures the StrongArm SnA signal is tied low.

Switching to CPU Idle

When is entered by disabling clock switching and performing a load operation from a noncacheable location and the Digital Controller then stops clocking MCLK. Normal operation is resumed by restarting MCLK.

Switching to CPU Sleep

To enter sleep mode, nRESET must be asserted for at least 20 ns and assert nPWRSLP, then switch off VDD, the supply to the core. The power to the StrongArm I/O drivers remains on.

To exit sleep mode, VDD is restored and nRESET and nPWRSLP are deasserted. The N2 platform's Digital Controller drives nPWRSLP with PowerEnable and nRESET. nPWRSLP is driven by the PowerEnable signal from the Digital Controller.

Core Clock Configuration

The high speed Core clock frequency is configured at reset by the four Core Clock Configuration pins. The N2 platform configures the Core Clock Configuration pins to allow the device to run at either 99.4 Mhz or 161.9 Mhz. To speed select between the two speeds, a resistor is loaded in either location R116 or R117. If the resistor is in location R116, the N2 device operates with a Core Clock of 99.4 Mhz. If R117 is loaded, the N2 device operates at 161.9Mhz.

Memory Clock Configuration

The N2 device configures the StrongArm to use external clocking by tying the SnA signal on the StrongArm and supplying MCLK to the StrongArm. MCLK is generated by the Digital Controller. As a result, all MCCFG signals are tied to ground.

Bus Interface

The N2 platform requires that the StrongARM CPU operate in Standard mode. In Standard mode, the full byte address is presented on the Address lines A[31:0], the line fills are not wrapped (so all burst accesses are guaranteed to begin at cache block word 0), and the write buffer only merges stores from store multiple instructions and castouts.

Read Data is always returned on the correct byte of the data bus D[31:0]. Write Data, presented to the Data Bus by the StrongARM, is placed on the byte lane specified by the two low-order address bits A[1:0]. The StrongArm does not replicate byte stores to all four bytes of the address bus.

Not all of the signals described in the following sections are accessible from the various connectors, but they are described in detail to provide you with additional information when using those connectors.

StrongArm Access Cycles

The StrongArm Bus interface is controlled by MCLK, and all timing references are with respect to MCLK. The speed of memory accesses on the N2 platform are controlled by the Digital Controller. To increase the access time to devices, the low phase of MCLK is stretched.

The StrongArm nWait signal is not used and is tied high.

Cycle Types

The StrongARM can perform two types of cycles: idle cycles and sequential cycles. These cycles are combined to perform memory accesses, and are differentiated by the pipeline signal nMREQ.

nMREQ is pipelined and so the value determines what type of cycle will follow. nMREQ becomes valid during the low phase of the cycle that precedes the one to which they refer. When nMREQ is low, the following cycle is a sequential cycle. When nMREQ is high, the following cycle is a idle cycle.

The address from StrongArm becomes valid during the high phase of MCLK. It is also pipelined, and its value refers to the memory access that follows it.

Memory Access

Memory accesses can be non-sequential or sequential. Non-sequential cycles occur when a new memory access is performed. Sequential cycles occur when the current memory access is of the same type as the previous access and the address is four bytes greater than the previous address, or during cache line fills. Cache line fills result from a cache miss to a sequential address and are distinguished from other bursts by asserting the CLF signal.

Non-sequential accesses are composed of an idle cycle followed by a sequential cycle. The address remains valid during the idle cycle to allow extra time for memory decoding. Sequential accesses consist of one sequential cycle.

Memory accesses can be read or write (determined by nRW) and will not change during a sequential access.

Address Pipe Enable

Address Pipe Enable (APE) is generated by the Digital Controller and is used to control the timing of the address signals, including A[31:0], MAS[1:0], nRW, CLF and LOCK. When APE is asserted, these signals will change when MCLK is high. When APE is deasserted, they will be held to the next MCLK low.

On the N2 platform, APE is configured to remain deasserted at all times.

Memory Access Types

The following diagrams show a one word read and one word write access, a two word sequential access, two one-word accesses back to back.

Figure 1-4 One-word Read or Write

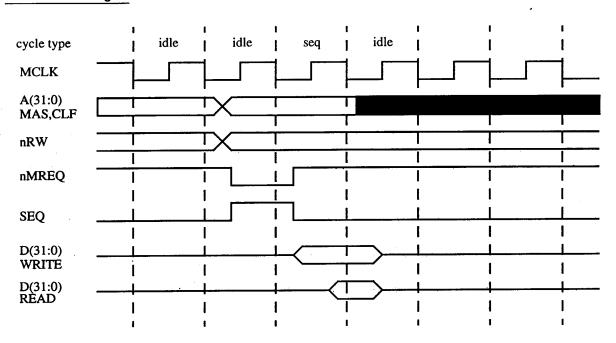


Figure 1-5 Two-word Sequential Read or Write

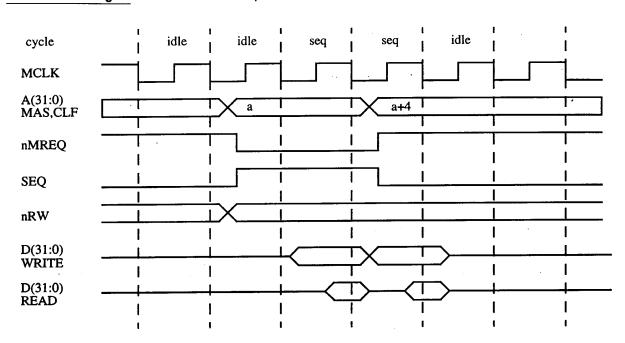
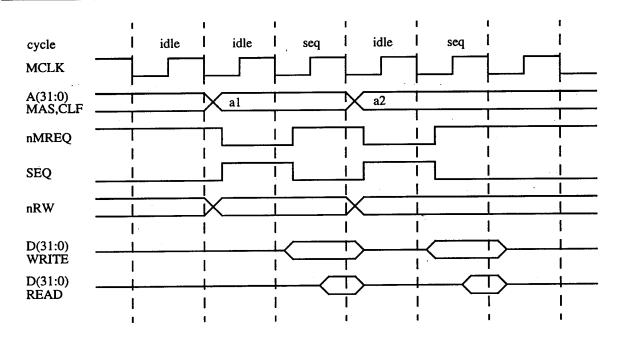
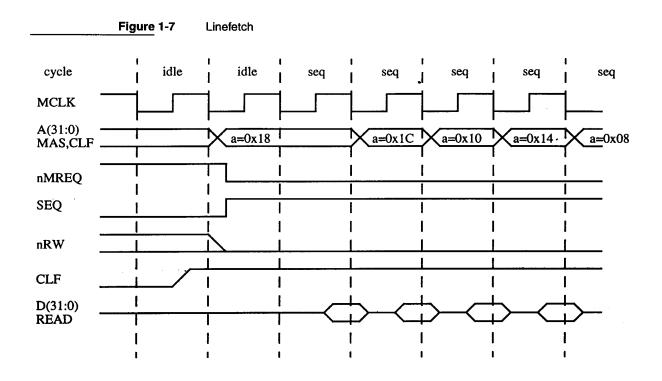
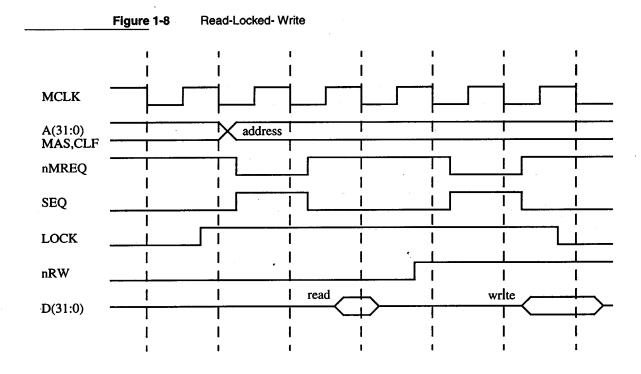


Figure 1-6 Two one-word Non-sequential Reads or Writes Back-to-back



1-18



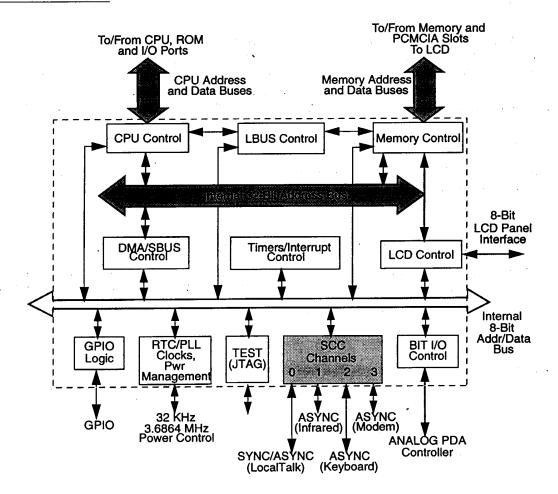


Digital Controller

The CL-PS7010 Digital Controller contains an 8-Channel DMA controller, an Interrupt Controller, an LCD Controller, and a 4-channel Serial Communications Controller (SCC), General Purpose Input/Output subsystem, Memory Controller, Timers and Real Time Clock, CPU and System Clock Generation, and Power Management State Machine.

This controller also provides bus interfaces to the StrongARM CPU, the two PCMCIA Controllers, and to the Analog Controller (via the Bit I/O bus). See Figure 1-9 for a functional block diagram of the digital controller.

Figure 1-9 Digital Controller Functional Block Diagram



CPU Interface

The CPU bus provides a direct connection to the StrongARM CPU, operating in Standard Mode. The CPU bus consists of a 32-bit data bus and a 32-bit address bus. All data transfers are synchronous and are clocked by the digital controller's memory clock

(MCLK), which can then be slowed down or shut off under software control to conserve power or to stretch access cycles. All MCLK stretching occurs when MCLK is low. MCLK, unstreched, operates at a frequency of 12.44 Mhz

Data transfers are latched on the falling edge of MCLK, and are initiated by the assertion of the memory request signal (MREQ) on the previous cycle.

The N2 ROM board also uses a subset of this bus to connect the Newton OS ROMs, Licensee ROM extensions, External I/O devices and additional FLASH user storage to the system. A description of that subset is described in Chapter X, "ROM Board Designer's Guide."

Memory and External I/O

The Newton OS ROMs, Licensee ROMs, External I/O devices and additional FLASH are connected to the system through a subset of the CPU Bus, accessible through the Mother Board's 72-pin ROM SIMM Connector. All accesses are intiated by the StrongARM. The Digital Controller decodes the address and generates the appropriate chip select signal. The Digital Controller supports six decoded address areas by generating six different chip selects. The following sections describe how the N2 device uses the chip selects.

Newton OS ROM Chipselect, ROM_CS_0

The Newton OS ROMs are decoded at address 0. They must be 32-bits wide and can be a maximum of 16Mbytes. ROM_CS_0 indicates that this space is being accessed by the StrongARM.

License ROM Chipselect, Additional FLASH, External I/O

The CPU bus also supports an external I/O area, decoded by ROM_CS_1, and can also be accessed through ROM. This area must be 32-bits wide and can be used for either Licensee ROM Extensions, Additional System FLASH, or External I/O devices.

LCD Backlight Control

The N2 device uses one of the available chip selects to control LCD Contrast. The chip select is connected to a 8-bit latch to provide

We had a hiccup here. The sentence above got cut off and the following sentence has nothing to do with backlighting.

The system PCMCIA Controllers, DRAM and Mother Board FLASH are connected to the system through the memory bus.

DMA Subsystem

The Digital Controller has a centralized DMA Controller that supports 8 DMA channels. DMA can occur from the Serial Port 0, Serial Port 1, Serial Port 3, Audio and the Tablet. All channels operate independently. Each DMA channel has its own long-word-aligned buffer that can be a maximum of 64K bytes.

The DMA Controller has a set of 4 registers (DMA Controller Registers) that control its overall operation. Each DMA Channel has a set of seven registers that configure the channel's operation and its buffer.

Abrbitration and Priority

The DMA Controller supports a fixed channel priority. Channel 0 has the highest priority and Channel 7 has the lowest priority.

Arbitration and selection among pending requests from the DMA channels occur only when the DMA controller is idle (no DMA accesses are in progress).

Once the DMA Channel arbitration has completed, the winning channel arbitrates with the LCD Controller and the CPU for access to the memory.

System priority, from highest to lowest, is as follows:

- 1. The DMA Controller with both Channels 0 and 1 enabled
- 2. The LCD Controller
- 3. The CPU (if the DMA Controller is currently accessing memory or has accessed during the memory 1 internal clock period before the CPU)
- 4. The DMA Controller
- 5. The CPU

2.2.3.2 DMA Controller Registers

The DMA Controller has 4 registers that control its operation. These registers are the Channel Assignment Register, the Enable Register, the Disable Register, and the Word Status Register.

2.2.3.2.1 Channel Assignment Register

The DMA channels are assigned physical devices, using the DMA Channel Assignment Register. The N2 platform is statically configures the Channel Assignment Register to assign the following devices to the Logical DMA channels:

Channel 0 - Serial port 0 Recieve,

Channel 1 - Serial port 0 Transmit

Channel 2 - Infrared (Serial port 1) Recieve and Transmit

Channel 3 - Audio Transmit

Channel 4 - Audio Receive

Channel 5 - Tablet Digitizer Receive

Channel 6 - Modem Port (Serial port 3) Receive

Channel 7 - Modem Port (Serial port 3) Transmit

2.2.3.2.2 Enable Register

The Enable Register allows individual DMA Channels to be Enabled only. It also is used as a status register allowing the N2 platform to determine if a given DMA channel is enabled or disabled.

A DMA channel is automatically disabled and the corresponding bit is cleared once DMA has completed for that channel or DMA has been disabled. The conditions causing Automatic Disabling are described in the Disable Register Section.

2.2.3.2.3 Disable Register

The Disable Register allows individual DMA Channels to be disabled. Using this register, the N2 Platform can abort DMA operations in progress for a given channel. A transfer in progress will be completed before the channel is disabled.

Once a DMA operation is disabled by using this register, it must be enabled again and DMA will continue where it was halted by the writing to the Enable Register. The Enable Register should be checked to ensure that the Channel is indeed disabled before enabling it.

Automatic DMA Disabling occurs on one of the following conditions:

- 1. Wrapping is disabled and the Count Register decrements to 0
- 2. The Size Register decrements to 0
- 3. Channel 0 recieves an End of Frame from the SCC Channel 0.
- 4. Disabling the DMA Channel by writing to the Disable Register.

2.2.3.2.4 Word Status Register

The Word Status register is read to determine if a DMA channel's Word Register contains valid data.

Once a DMA Channel's operation has beed disabled, this register must be read to deterimine if any valid residual data remains in the DMA Channel's Word Register. If valid data remains, the corresponding DMA Channel's Word Register must be read to complete the DMA operation.

2.2.3.3 Channel Register Organization

Each DMA channel has seven associated registers. These registers are the Base Register, the Pointer Register, the Size Register, the Count Register, the Control Reigister, the Compare Register, and the Word Register.

Newton Architecture Components

All DMA registers can be read at any time, including when the DMA Channel is active.

2.2.3.3.1 Control Register

The Control Register is used to configure the DMA Channel. The N2 platform configures the DMA channels differently, depending on the how they are assigned.

2.2.3.3.2 Base Register

The Base Register specifies the physical start address of the DMA buffer. This physical address must be long word aligned. This is accomplished by writing the register with 0 in the two low bit locations. The Base Register can also be used to specify the next buffer location to chain multiple DMA buffers.

2.2.3.3.3 Pointer Register

The Pointer Register is loaded with the starting address of the DMA buffer in Memory. This value may be the same as the Base Register, but can also be a location in the middle of the buffer and then, when the end is reached, wrap to the start of the buffer.

The Pointer Register is incremented by 4, One Long Word, each time the DMA controller accesses a word in Memory and stores it in the Word Register.

If Wrapping is enabled, this register will be loaded with the value of the Base Register when the end of the Buffer is reached. This allows implementation of singular circular buffers or chained Buffers. This register can be read at anytime to find the next buffer location to be accessed by DMA.

2.2.3.3.4 Count Register

The Count Register specifies the number of bytes remaining to be transferred. This register is intialized with the number of bytes to transfer.

The Count Register is decremented by one each time a byte is transferred to or from the Word Register to a Device. If Wrapping is enabled, the Count register will be loaded with the value in the Size Register.

2.2.3.3.5 Size Register

The Size Register can have two different uses, depending on how the DMA channel is configured:

The size register can be configured so that it represents the size of the DMA memory buffer in bytes. In this case, the size register value does not change and will be loaded into the Count Register if it reaches zero and a Wrap occurs.

The Size register can also be configured so that it represents the size in bytes of a DMA packet. This Packet may wrap in the DMA buffer if Wrapping is enabled. In this case, the DMA size register is decremented by four each time the DMA Controller accesses a word in memory and stores it in the Word Register. When the Size register decrements to 0 and the Word Register is empty, all subsequent requests from a device are ignored.

2.2.3.3.6 Word Register

The Word Register is used by the DMA engine to gather bytes transferred to and from DMA devices and convert them into words for transfering to and from memory.

During a transmit operation, a Long Word is read from the DMA buffer in memory into the Word register. The DMA controller then sends individual bytes or words to the device until the Word register is emptied. The next DMA transfer will then cause the DMA engine to perform another long word memory access to refill the Word register.

During a recieve operation, a byte or word from the device are gathered into the Word Register until it contains a Long Word. Once the register is full, the Word Register is written to the DMA memory Buffer.

A special case occurs for DMA transfers that do not have a modulo four number of bytes.

In this case, the word register may contain additional bytes that have not been transferred to memory. These bytes need to be transferred under Software control.

2.2.3.3.7 Compare Register

The Compare Register can be loaded with a value used to generate an interrupt when the Size register equals that value. The compare occurs after each DMA transfer.

2.2.4 LCD Subsystem

The Digital Controller has a built in LCD Controller that performs most of the LCD Subsystem functionality. This controller can support both dual scan and single scan Monochrome STN panels.

2.2.4.1 LCD Controller

The LCD controller can directly drive either 4-bit or 8 bit STN panels. These panels can be either Single or Dual Scan. The Main Logic Board's LCD connector provides a direct interface to the LCD controller and is described in the LCD Interface Designer's Guide Chapter.

2.2.4.2 Memory Organization

The LCD Controller operates from a Display Buffer stored in system DRAM. The organization of that buffer is in packed pixel format. The format of pixels within a byte are in Big Endian Format. Depending on the programmed number of bits per pixel value, the LCD controller consumes that many bits at a time to display a pixel.

The Display memory must be contiguous. In 4 bits per pixel, each byte represents a 2 pixels. In 2 bits per pixel, each byte represents 4 pixels and in 1 bit per pixel, each byte represents eight pixels. The following figure shows the display buffer organization for

2.2.4.3 Register Descriptions

The LCD Controller is configured through registers, described below.

2.2.4.3.1 Resolution Display Register

This register is used to program the panel's horizontial and vertical resolutions. These values are used by internal counters, which start at 0. A panel with HxV resolution, has H horizontial scan lines, numbered 0 to H-1 and V pixels in that scan line, numbered 0 to V-1. Therefore, the values programmed should be H-1 for the horizontial value and V-1 for the vertical value.

Dual Scan panels require that the vertical resolution be programed to half of the panel's actual resolution. A Dual Scan panel with HxV resolution should be treated as a panel with V/2 resolution. Therefore, this register should be programed with H-1 for the horizontial value and V/2 - 1 for the vertical value.

2.2.4.3.2 RMCLK Control Register

2.2.4.3.3 Main Clock Control Register		
2.2.4.3.4 ACMOD Control Register		
2.2.4.3.5 Power Sequence Time Constant		
2.2.4.3.6 Power Sequence Control Register		
2.2.4.3.7 Panel Interface Configuration Register		 *:
2.2.4.3.8 Gray Shading Control Register		
2.2.4.3.9 LCD Gray Shade Map Register		
2.2.4.3.10 Special Control Register	•	 1.
2.2.4.3.11 Horizontal and Vertical Retrace Reg		

2.2.5 SCC Support

The Serial Communications Controller (SCC) logic supports four serial channels (Channels 0 -3). Each channel supports full duplex operation, can be run in

asynchronous mode, and each has its own transmit and receive queues. The four serial channels are defined as follows:

Channel 0 is a high-speed interface with modem controls and Ring indicator.

Channel 1 provides a low-speed asynchronous link for IR communication.

Channel 2 provides a low-speed channel for printer support.

Channel 3 provides a channel for modem communications.

The features of each channel are listed in Table 1-2.

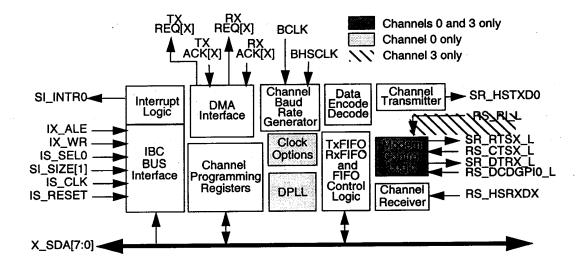
Table 1-2 Channel Features

Table to be supplied

2.2.5.1 SCC Hardware

Each SCC channel has supporting hardware that consists of a pair of transmit/receive FIFOs, an error FIFO, a DMA interface, abaud rate generator, and interrupt logic. Channel 0 has two additional logic blocks: a Digital Phase-locked Loop (DPLL) and some clock option logic. Figure 1-6 illustrates all of the SCC channel logic.

Figure 1-10 SCC Functional Block Diagram



Each channel's Transmit FIFO (Tx FIFO) is four bytes deep and can be programmed to flag the interrupt logic when either 1, 2, or 4 bytes are empty. This "threshold" is programmable. The Receive FIFOs (Rx FIFO) for channels 1 through 3 are also four bytes deep and have the same programmable thresholds as the transmit FIFOs. They will flag the interrupt logic when they are 1, 2, or 4 bytes full. Channel 0's Receive FIFO can be configured as either 3 or 4 bytes deep, so its threshold can be set to 1, 2, 3, or 4 bytes. The depth of this FIFO is also programmable.

Each of the four Receive FIFOs has a corresponding Error FIFO (Rx Error FIFO). The Error FIFOs are four bits wide and their depths match their respective Receive FIFOs. For each data byte in the Receive FIFO, a nibble is loaded into the Error FIFO that contains the Special Receive Condition status for that byte.

The DMA interface has two registers, Tx_Cmd and Rx_Cmd, that control separate enable lines for the transmitter and the receiver. When either the DMA transmit line (Tx DMA) or DMA Receive line (Rx DMA) is enabled, a request to the DMA controller is generated whenever the byte threshold of that channel's Transmit or Receive FIFO is reached. The resulting DMA transfer is done in a 1-, 2-, or 4-byte burst, as determined by the FIFO threshold.

Channels 1-3 have combination transmit/receive baud rate generators. Channel 0 has a pair of programmable transmit and receive baud rate generators, Tx BRG and Rx BRG. Each generator consists of a 16-bit down-counter.

The SCC interrupt logic consists of a register set that is used to set interrupt parameters and to capture information about an interrupt. They determine whether the interrupt is set on the rising or falling edge of a pin, which interrupt sources are masked or cleared, and record transitions on any of the interrupt pins. All of the interrupt lines are combined to produce a single interrupt. See the Section "Interrupt Support" for more information about the interrupt logic.

The Digital Phase Locked Loop (DPLL) is unique to Channel 0, and is used to recover Receive Clock information from NRZ1-, FM0-, or FM1-encoded data streams. The various clock sources and mode selection for the DPLL logic are programmable.

Channel 0 also contains clock option logic. This logic allows the transmit and receive clocks to be sourced from either the CTS pin, the DCD pin, the Tx BRG output, or the output of the DPLL.

GPIO Interface

There are 11 General Purpose I/O ports. The first ten, GPIO0-9, are available for assignment to external I/O devices.

In the N2 platform, the General Purpose I/O pins are assigned as follows:

GPIO0 - Configured as an input for the PowerSwitch

GPIO1 - Configured as an input to determine whether a AC Adaptor is installed

GPIO2- Configured as an input to determine the state of PCMCIA card lock $\boldsymbol{0}$

GPIO3 - Configured as an input to determine the state of PCMCIA card lock 1

GPIO4 - Configured as an output to control the 5 Volt Power Supply

GPIO5 - Configured as an output to control the 12 Volt Power Supply

GPIO6 - Configured as an output to shut down the LTC 1323 line driver

GPIO7 - Configured as an output to enable Fast Battery Charging

GPIO8 - Configured as an input to read IR FORM BUSY

GPIO9 - Serial Not CP Enable

In addition to the General Purpose I/O signals, the Analog controller supports 5 Digital Input/Output signals. These signals are configured as:

DIO0 - Input - Dock Attached

DIO1 - Input - Battery Not Charging

DIO2 - Available for configuration to the slot.

DIO3 - Turn on 5Volts to the PCMCIA Slot

DIO4 - Reset the IR Transciever

DIO5 - Input - Determine wheter a rechargeable battery Pack is installed.

Table to be supplied

2.2.10 Timer and Real Time Clock

The Digital Controller has a built in Real Time Clock with alarm used for all of the N2's time keeping functions. The Digital Controller also has 4 timers that are used by the Newton Operating System. Both of these are described below.

2.2.10.1 Real Time Clock

The Digital Controller has an accurate and stable 32.768 clock oscillator used to generate the Real Time Clock. The oscillator is driven by an external 32.768 crystal. The internal 32.768 clock is divided down internally to 1 Hz. The precision of the 1 Hz generator also includes circuits to digitally trim the 1 Hz frequency positively or negatively to provide accurate time to the N2 system. The trim values are determined at time of manufacture and stored in the N2's flash. The Real Time Clock's registers are described below. A diagram showing the Real Time Clock's clocking and registers is shown below.

2.2.10.1.1 Calendar Register

The 1 Hz clock is used to clock a 32 bit Counter that is stored in the Calendar Register. This register is used to keep the time in seconds.

2.2.10.1.2 Alarm Register

To generate an alarm, the absolute value in seconds is placed in the Alarm Register. When the Calendar Register matches the Alarm Register Value, an interrupt is generated.

2.2.10.2 Timer

In addition to the Real Time Clock, the Digital Controller also has a 32 bit Timer that is clocked by SCLK. The Timer is disabled in any power state where SCLK is disabled as described in the Power Management Section. Associated with the Timer are 4 match registers that are compared to the Timer to generate an interrupt. The Timer's registers are described below. A diagram showing the Timer's clocking and registers is shown below.

2.2.10.2.1 Timer Value Register

This register reflects the value of the 32 bit Timer.

2.2.10.2.2 Match Registers

There are 4 match registers that can be intitalized with different values. When the value of the Timer matches one of the four register values, an interrupt is generated. The interrupts caused by the timer matching the contents of the match register can be disabled.

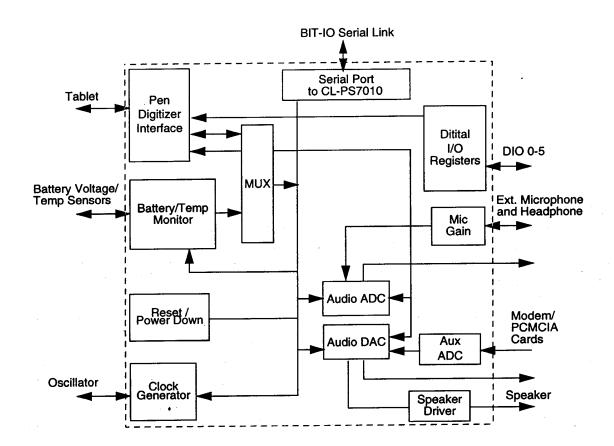
Table 1-1 Table 1-3 General Purpose I/O Ports

2.3 Analog Controller/Interface

The CL-PS7020 Analog Controller performs most of the N2's analog functions. The CL-PS7020 contains a tablet interface, battery and temperature monitors, a clock generator, audio A-to-D and D-to-A converters, microphone inputs, a speaker driver, and general-purpose digital I/O pins. This is a mixed-signal chip, combining both analog and digital functions.

Figure 1-7 shows the principal logic blocks that make up the CL-PS7020 Analog Controller.

Figure 1-11 Analog Controller Functional Block Diagram



All of the analog controller's internal functions are controlled by a set of registers located in the CL-PS7010 Digital Controller. Communication between the analog and digital controllers is over the BIT I/O interface, as described in the previous section.

2.3.1 Audio Support

The Analog Controller provides inputs for two microphones, two PCMCIA cards, and a modem. Outputs include a speaker and headphones.

The CL-PS7020's input logic supports both an internal and external microphone. One of the two input channels (MICIN1, MICIN2) is selected by an internal multiplexer. The signal from the selected channel is filtered and input to a 12-bit A-D convertor. The converter's output is then passed to the Digital Controller as a write command over the BIT I/O interface. The Analog Controller is the timing master during these transactions.

Both the gain and the sampling rate of the A-D converter are adjustable. However, if this converter is operating at the same time as the D-A converter in the output logic, the D-A converter controls the sampling rates of both.

The output logic can receive signals from either the Digital Controller, or from one of three auxiliary inputs.

Data from the Digital Controller comes over the BIT I/O interface to a level adjustment stage. The adjustment stage can modify the attenuation of the output in 63 steps of 2.498 dB each. The attenuated signal is routed to a D-A converter, and the analog output sent to either the speaker drivers (SPKROUT+, SPKROUT-), or to the drivers of an auxillary output (AUXOUT+, AUXOUT-) generally connected to headphones.

The CL-PS7020 begins the digital-to-analog conversion by issuing a read command to the Digital Controller. The Digital Controller replies with a write command containing the data.

The three auxillary audio inputs (AUXIN1-3) are typically connected to the modem speaker output and to PCMCIA cards. Each input is filtered, and passed to an auxillary A-D converter. The digitized signal is sent to a level adjustment stage, where the signal can be attenuated up to 18 dB, in three 6-dB steps. The attenuated signal is then mixed with the signal from the BIT I/O interface, and routed to either the speaker drivers or to the auxillary (headphone) output drivers. Both drivers are differential and may be selected independently of each other. The speaker driver is connected to an 8-ohm speaker, and the auxillary driver may be connected to any line-level input with an impedance of more than 1Kohms.

Tablet Interface

The N2's touch screen is a resistive style pen-digitizer tablet made up of two layers of conductive material. The first layer is applied to a sheet of glass protecting the display. The second layer of conductive material is applied to the underside of a flexible membrane that makes up the outer skin of the tablet, and is positioned over the first layer. When the pen is pressed against the outer skin, the two layers are brought together.

The CL-PS7020's interface to the tablet consists of seven lines: Two X-axis connections (TABXH, TABXL) are made to the right and left sides of the flexible membrane, and two Y-axis connections (TABYH, TABYL) are made to the top and bottom of the glass. The CL-PS7020 adjusts the voltages to these pins so that voltage gradients are formed across the X and Y axis. The outputs from the four pins are sent to individual channels of a 12-bit A-D converter. By measuring the voltages, the controller determines the point of contact where the two layers of the tablet are brought together by the pen. A fifth line, TABIN, is provided for five-wire digitizers. The last two signals, PRESDRV1-2, are used to measure pen pressure on the tablet.

Clock Generator

The CL-PS7020 uses a 3.6864 MHz crystal to generate the System Clock (SCLK) for the Digital Controller. The crystal is connected between the XTALOUT and XTALIN pins, which are, in turn, connected to a clock oscillator. The output of the oscillator, SCLK, is sent directly to the Digital Controller over the BIT I/O interface. SCLK is also sent to a phase-locked loop, and the output used to generate internal clocks for the CL-PS7020.

The clock oscillator has two modes: normal and low-power. In normal mode, the accuracy of the clock frequency to the crystal frequency is good, and the power consumption is moderate. In low-power mode, the frequency accuracy is reduced, but so is the power consumption.

Battery and Temperature Monitors

The battery voltage logic has two input lines, BATIN1 and BATIN2, which provide the main and backup battery voltages, respectively. Both lines are input to an A-D measurement converter that also multiplexes the signals.

The temperatures of the main battery and the LCD are measured using a pair of external thermistors. The thermister values (TEMPIN1-2) are both input to an A-D converter/multiplexor.

Digital I/O Support

The CL-PS7020 has six general-purpose digital I/O pins (DIO0-5). All six pins are bidirectional; their directions programmed through a direction register. Any of these lines may be set to generate an interrupt whenever the AINT signal to the Digital Controller goes high.

PCMCIA Controller Chip

The CL-PS7030 PCMCIA Controller provides the interface between a single PCMCIA card and the Digital Controller, and is compatible with PCMCIA Rev. 2.01. The N2 architecture supports up to four PCMCIA slots, each requiring its own CL-PS7030. The PCMCIA controller(s) provides translation buffers and latches, as well as support for DMA, both 3V and 5V PCMCIA cards, and hot card insertion/removal.

The CL-PS7030 supports these PCMCIA card configurations:

Memory-only (flash memory or SRAM)

I/O (such as a modem card)

A combination of both memory and I/O

DMA-capable

PCMCIA Interface

Data passes between the PCMCIA card and the Digital controller over one half of the 32-bit Memory Data bus. This bus is shared by the two PCMCIA controllers, DRAM, and flash memory. 26-bit addresses and 16-bit data words are multiplexed on either the upper or lower 16 bits of the bus.

Because PCMCIA addresses are 26-bits, two clock cycles are needed to transfer one address. The first ten bits are sent on the first clock of the Chip Enable (PCE_L) and the remaining sixteen bits are transferred during the second clock cycle. If the address is for

a write transfer, the write data is sent during the third clock cycle. If a word is being written, then write data is also sent during the fourth clock cycle of PCE_L. During read operations, read data is sent over the bus on the first, and sometimes second, clock cycles of the Chip Enable.

Each PCMCIA slot requires a General Purpose I/O (GPIO) pin to be used as the indicator for the PCMCIA card lock switch. The current architecture uses the following GPIOs:

CardLockSwitch0 - GPI/O2

CardLockSwitch1 - GPI/O3

Each of the PCMCIA card slots are allocated 256MB of memory space. Memory is allocated as follows:

PCMCIA Slot 1 - 256Mb @3000 0000

PCMCIA Slot 2 - 256Mb @4000 0000

Each slot's 256 Mbytes are equally divided into attribute space, I/O space, memory space and register space. The subdivision map is shown below:

Slot x Attribute Space -X000 0000 to X3FF FFFF

Slot x I/O Space - X400 0000 to X7FF FFFF

Slot x Memory Space -X800 0000 to XBFF FFFF

Slot x Register Space -XC00 0000 to XFFF FFFF

DMA Transactions

Because all of the PCMCIA card space is memory-mapped, the cards can be accessed directly by the CPU or by the Digital Controller's DMA logic. DMA operations can be either a memory-to-memory move, or an I/O-to-memory move. In both cases, the CL-PS7010 sees the PCMCIA controller as a memory element.

The PCMCIA controller sends the CL-PS7010 a Request Status signal (PDREQ_L) that can be used to handshake with the DMA controller.

DS2401 Serial Number Chip

The Digital Controller connects directly to the DS2401 Serial Number Chip with a one-line interface. This device contains a 8-bit family code, 48-bit serial number and 8-bit CRC. The device is read to obtain the 48-bit serial number used for product tracking.

2.2.X Power Management Subsystem

The Digital Controller has built in power management State machine. The Power Mangement Subsystem is responsible for minimizing and controlling the different subsystems and managing the power to the system. The power manager is controlled by both hardware and software state machines. The N2 platform's hardware is also designed to minimize current consumption. The sections that follow describe the Digital Controller's Power Management Subsystem.

2.2.3.1 Power Mangement Registers

The Digital Controller has a two registers that are used by the Newton Operating System to minimize the power on the N2 platform. These registers are the Power Management Register and CPU Control Register. Additionally, a number of the General Purpose I/O signals are used to control the power supplies on the Main Logic Board.

2.2.3.1.1 Power Management Register

The Digital Controller's Power Management Register is used to Enable of Disable subsystems. This register allows individual enabling or disabling SCC Port 0, SCC Port 1, SCC Port 2, SCC Port 3, the BIT I/O interface, the LCD Subsystem, and the DMA Subsystem. This register is also used by the Newton OS to place the system into the Sleep State.

2.2.3.1.2 CPU Control Register

The CPU Control Register is used to set the RUN state operating frequency of the Digital Controller's HSCLK. The register also configures the IDLE state operating frequency that clock.

The N2 platform configures the RUN state operating frequency to be 24.8832 Mhz and the IDLE state frequency to be 1/2 that value, or 12.44 Mhz. This register also contains a bit used to stall the StrongArm CPU's bus interface under software control by disablling the Digital Controller's MCLK.

2.2.3.1.3 Count Sheep Register

This Newton Operating System writes a value to this register to delay the Power Manager from entering the Comma State after a BFault or VFault.

2.2.3.1.4 Wakeup Register

A wakeup register is available to configure which Interrupt Sources can cause the system to wakeup. This register is described in more detail in the Interrupt Controller Section.

2.2.3.1.5 LCD Power Sequence Time Constant

This register allows the Newton OS to configure the amount of time between power control signals during power down and is described in detail in the LCD Controller Section

2.2.3.2 Power States and transitions

The figure below shows the state machine for the power manager in the N2 system. There are 7 states: Idle, Run, CountSheep, Coma, Sleep and Wakeup1 and Wakeup2. The power to the Digital Controller, which contains the power manager, is always on. Each of the Digital Controller's subsystems can be individually turned on and off under software control. A simplified State Diagram is shown below.

Power Management is controlled by two different Hardware generated signals: BFault and VFault. BFault, or Battery Fault occurs when the battery voltage drops below 3.7 Volts. VFault occurs when the Digital Logic Voltage, dvcc, drops below 3.0 Volts.

Additionally, the output signal PowerEnable from the Digital Controller is used to indicate to the system that the system is awake. When the signal is asserted, the system is awake or waking up. When the signal is negated, the system is sleeping. This signal is available for use on the ROM Simm Connector and its use is described in the Chapter Rom Board Designer's Guide.

2.2.3.2.1 IDLE State

The N2 system enters the idle state through software control. The Newton OS writes to a bit in the CPU Control register to pause the StrongArm Processor's Bus Interface.

In this state the Digital Controller stops MCLK flowing the conclusion of the current bus cycle that caused the idle condition. The Digital Controller is configured to reduce the frequency of the internal High Speed clock by 1/2 entering this state.

The Digital Controller continues to assert the PowerEnable in this state.

The detection of any enabled and unmasked interrupt will cause the Digital Controller to move to the RUN State and is normal path.

However, if BFault or VFault are detected, the system will immediately transition to the Coma State, powering down the system.

2.2.3.2.2 RUN State

The Run State is the normal operating state for the N2 device. When in the Run state, the StrongArm CPU Bus interface is clocked with MCLK. The Digital Controller's HSCLK is operating at the full frequency and the power supply is fully functional. The Digital Controller continues to assert PowerEnable in this state.

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Under control of the Digital Controller's Power Management Register, other software states may be entered which are identified by the enabling or disabling of internal and external subsystems as needed with either GPIO signals or using the Digital Controller's Power Management Register, including the Serial Port 0's Line Driver.

2.2.3.2.3 WakeUp 1 State

If the N2 system is in either the Sleep State, or the Coma State, an external event can attempt to wake the N2 system as long as there is sufficent battery voltage. The external events that can wake the system are described in the Coma State and the Sleep State.

When attempting to wake, the Digital Controller starts a 500 msec timer. The power supply must be stable, indicated by the absence of Vfault, within in this period of time or the Digital Controller will place the N2 Device in the Coma State.

If the power supply becomes stable earlier, indicated by the negation of Vfault, the device will enter the WakeUp 2 State.

If during this period a Bfault occurs, the system will enter the Coma State.

2.2.3.2.4 WakeUp 2 State

Once the power supply has attained the correct voltage, the Vfault signal will be removed. However, during this time, the power supply may be unstable, causing multiple Vfaults. To ensure that the system is not brought up before the power supply is stable, a 30 msec timer is started when entering this state. If no Vfault occurs during this period, the system enters the run state. If, during this period the power supply dips, and Vfault occurs, the system will enter the Wakeup1 State and remain there until the Vfault is removed. Once the N2's power supply is stable, the system enters the Run State.

If during this period a Bfault occurs, the system will enter the Coma State.

2.2.3.2.5 COMA State

The purpose of the Coma State is to reduce the number of events that can power up the system once a Bfault or Vfault has occured. The events that allow the system to try and wake up are Attention or GPIO 0 or GPIO 1. GPIO 0 and GPIO 1 can only cause the system to wake up if those interrupts have been enabled and are not masked. Therefore, even if other interrupts are programed to Wake the system, the N2 Device will remain in this state.

However, if BFault is still present, the N2 system will remain in the Coma State.

Attention is connected to the reset button on the Main Logic Board. GPIO 0 is connected to the Power Switch connector on the main logic board. GPIO 1 is connected to the AC adaptor detect signal.

When entering this state, the Digital Controller will initiate a hardware shutdown sequence. This sequence will power down the external LCD subsystem components by first negating DISP, the backlight control, and then VEE_Enable, the LCD Drive Voltage. The Digital Controller will then negate CLK_ON and PowerEnable, turning off the

system Clocks and the power supply. The LCD Modulation Clock ACMOD and VCC_EN will then be turned off after a programmable delay, specified by the Power Sequence Time Constant Register.

2.2.3.2.6 Count Sheep State

The Digital Controller's CountSheep Register provides a delay before the N2 system's Power supply is shut off by negating PowerEnable. This allows the Newton Operating System to clean up before the N2 Hardware is shutdown.

2.2.3.2.7 SLEEP

The Sleep State occurs when the OS sets the Sleep System bit in the Power register. In this mode, all clocks are disabled and all subsystems are shutdown, except clocking to the Digital Controller's Real Time Clock. Both HSCLK and SCLK are shut off to minimize power.

When entering this state, the Digital Controller will initiate a hardware shutdown sequence. This sequence will power down the external LCD subsystem components by first negating DISP, the backlight control, and then VEE_Enable, the LCD Drive Voltage. The Digital Controller will then negate CLK_ON and PowerEnable, turning off the system Clocks and the power supply. The LCD Modulation Clock ACMOD and VCC_EN will then be turned off after a programmable delay, specified by the Power Sequence Time Constant Register.

This state is exited by any enabled and unmasked wakeup interrupt. The system then enters the WakeUp1 state.